Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **C EXT 1**
2. **R EXT1/C EXT1**
3. **CLR1**
4. **B1**
5. **A1**
6. **Q1**
7. **N. Q1**
8. **GND**
9. **N. Q2**
10. **Q2**
11. **A2**
12. **B2**
13. **CLR2**
14. **R EXT2/C EXT2**
15. **C EXT2**
16. **VCC**

**.051”**

**.068”**

**1**

**16**

**15**

**4 3 2**

**5**

**6**

**7**

**8**

**9**

**10**

**11**

**12 13 14**

**MASK**

**REF**

**7**

**8**

**5**

**1**

**C**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 7851C**

**APPROVED BY: DK DIE SIZE .051” X .068” DATE: 4/25/22**

**MFG: FAIRCHILD / NSC THICKNESS .015” P/N: DM9602**

**DG 10.1.2**

#### Rev B, 7/19/02